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A programmable delay line

Abstract

The paper describes the design and test results of a programmable digital delay line implemented in an FPGA device (Kintex-7, Xilinx). The operation of the delay line is based on the modified dual interpolation Nutt method that combines two actions, i.e.: (1) counting the periods of a reference clock and (2) time interpolating within a single clock period. The first action provides an extremely wide range of the introduced delays (> 9 minutes), while the second one allows reaching relatively high delay resolution (2 ns) with a timing jitter as low as 35 ps (until delay of 1 μs). The high metrological parameters of the designed delay line are achieved at the expense of increased difficulty in implementation of the method in an integrated circuit. The major problems to be solved were the synchronizations of input signals as well as synchronous and asynchronous parts of the system, which were effectively provided with the use of two dual-edge synchronizers, a clock signal logic level detection system and associated synchronizers.

Keywords: delay line, dual interpolation method.

1. Introduction

Digital delay lines are currently commonly built as specialized integrated circuits in ASIC (Application Specific Integrated Circuits) CMOS technology [1]. This technology allows a lot of flexibility to design process and provides the possibility to achieve very high measurement resolution and precision. However, the design and manufacturing process is relatively long and expensive. In addition, integrated delay lines currently available have significant restriction consisting in the fact that the resolution of the line decreases with its delay (Tab. 1). An alternative technology to custom chips are programmable devices, especially FPGAs (Field Programmable Gate Array) [1] that can be reconfigured at any stage of the design process, which makes any amendments to the design faster and cheaper [1, 2]. A delay effective solution for this problem might be the use of a modified Nutt method, i.e. delaying the asynchronous pulses using an in-period interpolation of the reference clock signal. The paper describes the design and test results of a programmable digital delay line based on the modified dual interpolation Nutt method and implemented in an FPGA device.

Tab. 1. Basic parameters of selected delay lines

Device	Delay range	Delay resolution	Jitter [range]
MC10EP195	12.2 ns	10 ps	1 ps [10 ns]
SY89295U	14.8 ns	10 ps	10 ps [10 ns]
DS1045	84 ns	5 ns	-
DS1100	20 – 500 ns	4 – 100 ns	-
Ref. [7]	1 s	250 ps	250 ps [1us]
Ref. [8]	4.4 ms	65 ps	100~200 ps [1 us]
This work	550 s	2 ns	35 ps [1 us]

2. Method of wide range delay generation

Delay generation based on the modified dual interpolation Nutt method [3] involves counting the clock pulses ($N_C T_C$) and the two stage interpolation within a single period of the clock signal (Fig. 1).

The first interpolator, realized as a time-to-digital converter (TDC), accurately measures a time interval T_A between the moment of appearance of the input signal and the nearest active edge of the clock signal.

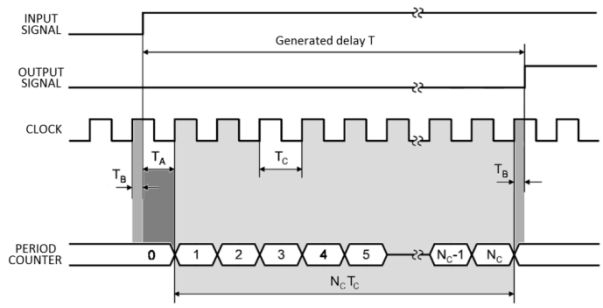

Fig. 1. The principle of delay generation in the modified Nutt method

The second interpolator, made as a digital-to-time converter (DTC), generates a time delay T_B, which is a difference between the clock signal period T_C and the time T_A.

$$T = T_A + N_C T_C + T_B \quad (1)$$

The accuracy of the system depends on the accuracy of the converters used (TDC and DTC). The proposed method enables delaying the input signal by the duration of a set number N_C of clock periods T_C. Moreover, this method reduces the counting method error ($\pm T$) to the much smaller value of errors in both converters.

3. Design of a programmable digital delay line

The block diagram of the designed programmable digital delay line is shown in Fig. 2.

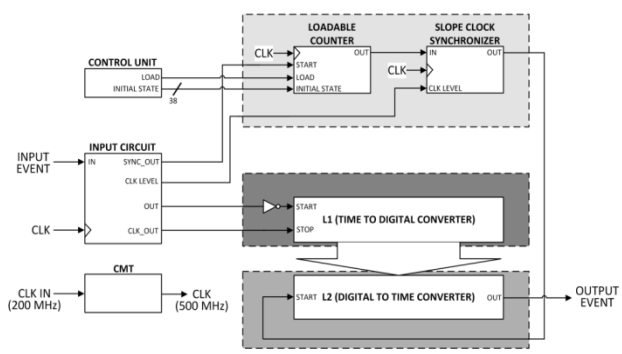

Fig. 2. Block diagram of the programmable delay line

In the project, an external clock signal (CLK IN) with a frequency of 200 MHz is used. The functional block CMT (Clock Management Tile) increases the frequency of the input clock signal forming the clock signal (CLK) with a frequency of 500 MHz. A synchronous loadable counter used in the project counts the periods of the clock signal with a resolution of 2 ns.

The maximum time that can be measured using this counter is:

$$t_0 = 2n/f \quad (2)$$

where the frequency f = 500 MHz, and the maximum number of bits n = 38. Thus the maximum possible time to be measured is about 9.16 minutes. The input signal is delayed by the number of periods of the clock signal predetermined in the control unit. The user-entered number of periods of the delay is propagated to the loadable counter at the time of system reset. At this time, the input circuit does not react to the input pulses. After the reset, the control unit activates all the blocks of the system, enabling receiving asynchronous pulses in the input circuit. The synchronized input pulse (SYNC_OUT) propagates to the input START of the loadable counter. This synchronization causes a time delay in relation to the asynchronous input pulse. The asynchronous input pulse (input event) propagates through the inverter [4] to the input of TDC (L1), starting a measurement of the time delay caused by synchronization. The value of this delay time is in the range from zero to the period of the clock signal. The operating range of converters (L1 and L2) covers half of the period of the clock signal (1 ns). With the arrival of the asynchronous input pulse, the logic level of the clock signal (CLK LEVEL) is tested. At the same time, the input pulse is synchronized to the first (rising or falling) edge of the clock signal. This signal is supplied to the STOP input of the converter L1. Data from the converter L1 are attached to the information of DTC (L2), which is waiting for the trigger signal to generate the time interval. The loadable counter is synchronized to the rising edge of the clock, and the converter L1 is synchronized to the rising or falling edge of the clock. Having measured a number of periods of the clock CLK, the output signal from the loadable counter propagates to the input of the slope clock synchronization block, in which it is synchronized to the rising or falling edge of the clock signal, depending on the level of the clock signal detected at the time of arrival of the input pulse (CLK_LEVEL). The signal from the synchronization block propagates to the input START of L2. The converter L2 generates a time delay TB, which is a difference between the clock signal period TC and the time TA, stored in the converter L1. If the data on the information input of the flip-flop change during the close proximity of the active edge of the clock signal, metastability effect may occur at the output of the flip-flop. It can introduce an extra propagation time and randomness in determining of a final state at the output of flip-flop. To eliminate the effect of metastability in the process of synchronizing, the input pulse to the first (rising or falling) edge of the clock signal is applied at the input circuit of a double double-edge synchronizer [5].A double synchronizer is built from two D flip-flops connected in series. At the time of occurrence of asynchronous data at the double synchronizer input and the double synchronizer timing clock signal at the first flip-flop output, metastability effect may occur. If, however, the period of the clock CLK is longer than the time to determine a final state at the first flip-flop output, then the signal at the synchronizer output is already deprived of the metastability effect.

The block of delay lines is built from two converters: time-to-digital (L1) and digital-to-time (L2). Each converter consists of 50 CLB (Configurable Logic Block). Multiplexers CARRY4 are used as delay elements. In both converters the falling edge is active [4]. During the experimental studies it turned out that the falling edge propagated for converters faster than the rising edge. For converter L1 the order to switch the flip-flops was experimentally set [6]. The system propagated the falling edge as well as set the order of switching the flip-flops. The obtained average resolution of the delay line block was 12 ps.

The digital programmable delay line was designed with the use of the system ISE Design Suite and implemented in a Kintex-7 (7K325T) device from Xilinx. The project occupies about 0.4% of logical cells, 10% of CMT (Clock Management Tile) blocks and 22% of global buffers.

4. Experimental research

Fig. 3 shows the graph of timing jitter of the delay time generated within a wide range. For time delays up to 100 μs the timing jitter is low and does not exceed 100 ps. However, for the longer delay times the obtained timing jitter increases and for 1 ms is 26 times higher (σ = 810 ps) with respect to the timing jitter value over a narrow range (< 10 μs). The primary cause of this phenomenon is the instability of the reference clock source [1] and the inherent jitter of the CMT block. Therefore, the use of an external frequency synthesizer with better parameters than internal CMT can reduce the jitter of the clock signal that drives the synchronous part of the system. However, this may lead to higher cost of the system.

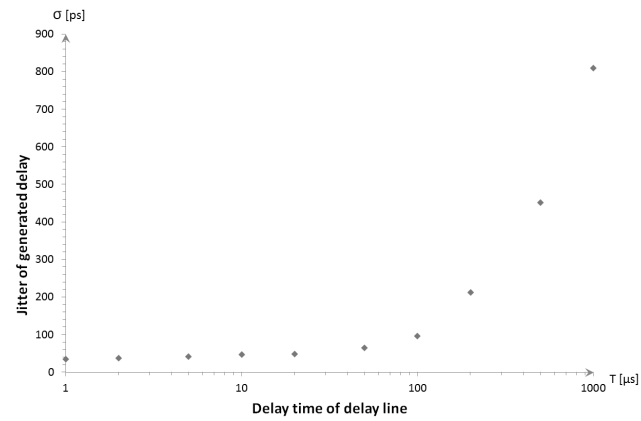

Fig. 3. Timing jitter of generated delays

The dead time of a delay line is the minimum time interval that elapses after the registration of the input pulse to the next pulse on the line input, which can be registered by a delay line. The dead time of the designed delay line depends on the input pulse duration, the minimum delay of the line, as well as the time needed to reset the whole delay line. The minimum dead time is approximately 128 ns.

FPGA-based implementation of the delay line creates possibility to relatively easy increase its parameters, such as the delay range and resolution. The former one can be extended by increasing the capacity of a binary counter, whereas the latter one may be improved by introducing an additional delay circuit to precisely delay the output signal within a narrow range of a single clock period (2 ns). For this purpose a digital-to-time converter may be implemented in the FPGA device or an external integrated delay device, e.g. MC10EP195 can be employed. It should be noted, however, that such improvement in the resolution may deteriorate the jitter of the entire system.

5. Summary

The designed and manufactured model of an integrated programmable digital delay line using of the modified Nutt method, implemented in an FPGA device is presented. The developed delay line provides an extremely wide range of introduced delays (> 9 minutes), the timing jitter as low as 35 ps until delay of 1 μs, the resolution of 2 ns, the minimum delay time equal to 24.4 ns and the minimum dead time of less than 128 ns.

Implementation of the designed delay line in the FPGA device allows integrating almost all parts of the system in a single integrated circuit that seems to be the most cost efficient solution.

The use of any external electronic parts, e.g. an additional frequency synthesizer, could improve the parameters of the system but at the cost of higher expense.

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6. References

[1] Carbone P., Kiaei S., Xu F.: Design, Modeling and Testing of Data Converters. Chapter 7, Szplet R.: Time-to-Digital Converters. Springer, 2014.
[2] Szplet R., Jachna Z., Kwiatkowski P., Różyc K.: A 2.9 ps equivalent resolution interpolating time counter based on multiple independent coding lines. Meas. Sci. Technol. 24, 2013.
[3] Nutt R.: Digital time intervalometer. Rev. Sci. Instr., vol. 39, no. 9, pp. 1342-1345, 1968.
[4] Szplet R., Sondej D., Grzęda G.: Bezpośredni przetwornik czas-liczba z kodowaniem wielokrotnym. Pomiary Automatyka Kontrola, vol. 59, no. 8, pp. 842-844, 2013.
[5] Szplet R.: Synchronizacja sygnałów w interpolacyjnych licznikach czasu. Biuletyn WAT, vol. 57, no. 4, pp. 285-308, 2008.
[6] Kwiatkowski P., Szymanowski R., Szplet R.: Identyfikacja parametrów dynamicznych linii szybkich przeniesień oraz globalnych linii zegarowych w układach programowalnych Spartan-6. Pomiary Automatyka Kontrola, vol. 59, no. 8, pp. 757-759, 2013.
[7] Li J., Zheng Z., Liu M. and Wu S.: Large Dynamic Range Accurate Digitally Programmable Delay Line with 250-ps Resolution. The 8th International Conf. on Signal Processing, vol. 1, pp.16-20, 2006.
[8] Song Y., Liang H., Zhou L., Du J., Ma J., Yue Z.: Large Dynamic Range High Resolution Digital Delay Generator Based on FPGA. In International Conference on Electronics, Communications and Control, pp. 2116-2118, 2011.

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