A New Methodology for Designing and Development of Complex Systems for High Energy Physics

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***Abstract*—The paper describes a new methodology that allows to design scalable complex control and data acquisition systems taking into consideration the additional, non-functional requirements of High-Energy Physics (HEP).**

Electronic systems applied in HEP often operate in difficult conditions. Access to such devices is difficult or even impossible. The HEP systems require high availability, serviceability and upgradeability. The operating conditions of these systems are even more difficult than for telecommunication devices. Therefore, a different methodology should be applied than for classical telecommunication systems, when designing electronics used in high-energy physics applications.

Electronic systems also need a suitable hardware platform that not only assures high availability, simplifies maintenance and servicing but also allows to use mixed analogue-digital signals.

The author made an attempt to develop a new methodology suitable for designing of complex data acquisition and control systems of HEP. The Low Level RF (LLRF) system of European Free Electron Laser (EXFEL) and Image Acquisition System (IAS) prototype developed for International Thermonuclear Experimental Reactor (ITER) tokamak are presented as examples of complex electronic systems that were designed according to the proposed methodology.

***Index Terms*—Design Methodology, High Energy Physics, Large Scale Systems, Electronic Systems, AdvancedTCA, MicroTCA, Reliability, Availability, Serviceability, Low Level Radio Frequency Control System, Image Acquisition System**

I. Introduction

ELECTRONIC systems applied in high-energy physics often operate in difficult conditions: in increased temperature and considerable dust. They are exposed to influence of intensified radiation and magnetic fields. In many cases, access to such devices is difficult or even impossible. The operating conditions of these systems are even more difficult than for telecommunication devices.

A different design methodology should be applied than for classical telecommunication or IT (Information Technology) systems, when designing electronics used in high-energy physics. For this reason, it is extremely important to develop effective RAS (Reliability, Availability, and Serviceability) methods, which provide remote diagnostics of the systems, prompt reporting of problems, anticipation of failures and providing a possibility of hot-swappable replacement of damaged parts.

Therefore, a suitable and elastic hardware platform is required that allows to use redundancy of critical subsystems such as power supply, cooling, data transmission interfaces and hardware management controller in order to improve the overall system availability. The platform should support straightforward hardware scalability, extension or upgrade using a modular architecture. In this way, the number of acquisition channels could be increased or the sampling parameters and/or data processing power could be enhanced.

Usually, the electronic systems are built using front- and rear-side modules installed in a chassis. Most of the signals are transferred via a chassis backplane, including main communication bus, interlock, trigger and timestamp signals needed in HEP applications. This allows to enhance device reliability and design complex scalable systems that could be easily extended by plugging new modules into the chassis.

Some systems allow to use a rear site modules for analogue signal conditioning [1]–[3]. Such an attempt facilitate analogue and digital domains separations and significantly improve analogue subsystem performance [1], [4]. Some standards even support a dedicated rear-side backplane that allow for distribution of sensitive analogue signals, reference RF frequencies, and clock signals [1], [4].

Another desired functionality in HEP is hardware management that simplify diagnostics and maintenance of devices installed in the chassis. The Hardware Platform Management (HPM) subsystem provides a hot-plug and hot-swap features and therefore make it possible to replace the faulty module during a normal operation without power or system shutdown [5].

Some telecommunications standards use the Intelligent Platform Management Interface (IPMI) mechanisms to manage and diagnose the devices installed in the chassis [2], [3], [6], [7]. The IPMI subsystem is responsible for a continuous monitoring of crucial system components' conditions, such as power supplies, fans in the cooling system, power consumption, voltages and currents or temperatures of the components in order to detect impending failures [5]. Certain symptoms, e.g. decreasing speed of a fan and increasing temperature in a certain part of the chassis could be recognized before the impending failure of the cooling system. Application of HPM subsystem, redundancy and proper response to alarm signals can significantly increase the whole system reliability and help to achieve availability as high as 99.999% (6 minutes of down time per year) [2]. The IPMI could also simplify diagnostics and servicing of HEP devices installed in the places with difficult and limited access, such as: accelerator tunnels, radiologically controlled or laser light areas and tokamak vaults.

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Electronic systems used in high-energy physics require a specific design and testing process. Very often, the machine or its components (e.g. accelerator infrastructure or tokamak vessel) are not yet available in the last stage of electronic system implementation and therefore it is not possible to perform the final tests of the built system. Because of this, the final tests have to be executed with application of a device model or a dedicated emulator[1] [8].

A part of the HEP systems is exposed to increased ionizing and non-ionizing radiation or magnetic fields. Therefore, a dedicated design methodology is required to develop systems that tolerate both Total Ionizing Dose (TID) and Single Event Effects (SEEs). The replacement of hardware components must be scheduled when the total allowed dose is achieved. The systems also require a suitable hardware platform that will operate in such conditions and support remote hardware diagnostics and replacement.

The research conducted by the author focused on finding new methods, procedures of building complex electronic systems, standards, circuit and software solutions, manners for diagnosing, remote management, maintenance and servicing of electronic devices working in difficult conditions of HEP. He has designed and participated in the construction of dozens of electronic devices prototypes developed in new technologies (Micro Telecommunications Computing Architecture: MTCA.4, MTCA.4.1) [3], [4], as well as modified telecommunication xTCA technologies (MTCA.0, Advanced Telecommunications Computing Architecture, Advanced Mezzanine Card) [2], [7], [9]. The experience gathered during constructing prototypes helped to develop the methodology.

For the purposes of the developed methodology, the author defines a complex system as a device that fulfils the following criteria:

1) acquiring and/or processing data from more than 100 analogue or 1000 of digital channels with a total data throughput higher that 160 Gbps (e.g. 100 channels with sampling frequency more that 100 MHz and 16-bit resolution),
2) acquiring and/or processing images from more than 10 cameras with a total data throughput higher that 80 Gbps (e.g. 10 digital 1 Mpx cameras with 1000 fps and 8-bit colour),
3) has a distributed architecture, uses more that two chassis, which requires a nanosecond synchronisation.

The paper has the following structure: Section II describes the methodology proposed by the author. Section III discusses selected hardware platforms suitable for designing complex system of HEP. Two examples of complex, scalable systems that follow the methodology are presented in the section IV, whereas section V contains summary and plans for the future.

II. Methodology to Design Control and Data Acquisition Systems of HEP

The concept for developing of complex scalable control and data acquisition systems methodology arose during the development of LLRF control device prototype for FLASH accelerator that was developed in VME Bus technology. The methodology has been verified practically by the author during further research concerning design and construction of LLRF system components for the FLASH as well as EXFEL linear accelerators and the prototypes of ITER (International Thermonuclear Experimental Reactor) tokamak diagnostic subsystems.

Following the methodology it is possible to build a complex, distributed system that meets not only functional requirements but also a number of specific non-functional requirements that have a significant influence on machine availability, reliability, serviceability and safety. It has also a direct influence on the success of physical experiments frequently worth several billion euros.

The foundations of the methodology were created during development of the prototype LLRF control system for the European-XFEL accelerator. The first prototype, built using the VME Bus technology, was able to control a single cryomodule (32 cavities) and therefore fulfils the functional requirements. However, the selected VME Bus technology has various limitations that prevent designing of a scalable enough system with high RAS.

Further research resulted in the design of pioneering prototype of the LLRF system using telecommunication AdvancedTCA standard [1], [10]–[15]. Finally, a new promising MTCA.4 (MicroTCA.4) specification dedicated for HEP applications was released [3]. The proposed methodology was applied by the author during the development of the components for the final EXFEL control system prototype [16]–[19].

The methodology was also applied during the design of scalable, high-performance Image Acquisition and processing System (IAS) prototype [20]. The IAS dedicated for ITER tokamak diagnostics, designed with MicroTCA.4, was built and evaluated. The IAS allow to process data with a terabit throughput, while the application of MicroTCA.4 assured scalability and high availability.

The new methodology proposed by the author for design and development of complex systems used in HEP experiments includes among others:

1) Analysis of control or data acquisition systems requirements; development of functional System Requirement Specification (SRS) and System Design Specification (SDS).
2) Analysis of system architecture taking into consideration the specific HEP requirements:
   a) Required data processing efficiency and its hardware implementation using internal or external devices such as: CPUs (Central Processing Units), GPUs (Graphics Processing Units) and FPGAs.
   b) The maximum latency in control loop or data acquisition path.
   c) The number of analogue, digital and vision channels.
   d) System modularity – its design with application of selected standards; mapping of the system into basic modules: chassis, font- and rear-modules, signal conditioning circuits, etc.

[1]In the case of the European X-ray Free Electron Laser (EXFEL), a prototype machine Free Electron Laser in Hamburg (FLASH) was constructed to verify the concept, test and evaluate various subsystems.

e) Required reliability and availability of the system, the redundancy on the following subsystems or interfaces: power supply, cooling, management, trigger and interlock, data transmission.
f) Required system scalability and the possibility for further extenssion or upgrade.
g) Hot-swappability of crucial components (power supply, cooling devices, and modules realizing system functionality).
h) Concerning operation in difficult conditions including high-temperature and limited possibility of heat dissipation, increased magnetic field and radiation (tolerance of ionising radiation, neutrons, protons, heavy ions and errors caused by their impact, e.g. SEU, SEE, etc.).
i) Long-term availability of applied solutions and used components[2]).
j) Possibility to connect crucial analogue signals from rear-side of the chassis.

3) Analysis and selection of the main interface for data transmission taking into consideration requirements, such as: data throughput, maximum latency, transfer protocol, communication model, topology (bus, star, full-mesh), possibility of switching and routing packets, etc.
4) Analysis and selection of the secondary interfaces for devices configuration, diagnostics, and management taking into consideration requirements, such as: data throughput, maximum latency, transfer protocol, communication model, topology (bus, star, full-mesh), possibility of switching and routing packets, etc.
5) Analysis of reference RF frequencies, precision clock signals, timestamps used in HEP systems, and possibility of their distribution using chassis backplane.
6) Analysis of analogue signals, in particular high-frequency signals, and possibility of their distribution using front-panels of front- and rear-site modules.
7) Analysis and development of the architecture of management and diagnostic subsystem (monitoring of crucial system components, power supply voltages and currents, temperatures, clock signals and other diagnostic parameters).
8) Analysis and development of remote methods for in-system firmware upgrade of programmable devices (microcontrollers, processors, FPGA, DSP devices) in the main and auxiliary systems, e.g. management-diagnostic subsystem, power supply or cooling devices, etc.

The methodology developed by the author covers the entire lifecycle of complex electronic systems (from concept to mass production, further use and servicing of the device), bearing in mind the specific aspects and requirements of large high-energy physics experiments. A significant number of HEP systems use programmable devices (FPGAs, microcontrollers, processors, DSPs, GPUs) and therefore a hardware-software codesign technique should be applied to verify the compatibility of firmware with designed electronic circuits. The proposed methodology for the design of complex electronic HEP systems consists of the following phases:

1) Collection of functional and non-functional design requirements for the electronic system.
2) Development of a high-level functional block diagram of the device.
3) Analysis of possible design including state-of-the-art solutions; development of the system architecture.
4) Development of a device prototype (iterative process repeated until the prototype meets the SRS requirements):
   a) Verification of selected system and software solutions: simulations, testing of device subsystems and selected software routines. Development of software procedures (low- and high-level) in order to verify it with the electronic circuit design (e.g., checking the compatibility of used FPGA resources with external electronics).
5) Construction of the device prototype:
   a) Development of low- and high-level software.
   b) Execution a detailed tests of built system in a laboratory.
   c) Integration of electronic system with the machine available in High-Energy Physics institution. Performance of real-life tests, e.g. using the machine hardware in an accelerator tunnel or device emulator (such as cavity assembled in cryostat), if the construction of the machine is not yet finished.
   d) Verification of system parameters compliance with design requirements.
   e) Construction of another prototype in case the built device does not meet the design goals.
   f) Design of the final device, including required corrections and modifications.
6) Construction of the final prototype:
   a) Upgrade and modifications of low- and high-level software.
   b) Evaluation performance and detailed tests of built system and its subsystems in a laboratory.
   c) Integration of electronic system with the machine available in High-Energy Physics institution and performance of real-life tests.
   d) Verification of system parameters compliance with design requirements.
   e) Development of a dedicated test-bench for automated testing of mass production devices.
7) Running a trial serial production:
   a) Verification of the electronic system and/or all electronic components of the system using an automated test-bench.
   b) Execution of detailed tests of the system or system components in the laboratory.
   c) Final verification of system parameters compliance with design requirements.

[2]One of the important, non-functional requirement of EXFEL accelerator LLRF system was a long-term availability of used components and devices (more than 20 years).

TABLE I
COMPARISON OF APPLICATION, ELECTRICAL AND MECHANICAL PARAMETERS OF SELECTED STANDARDS

	VME Bus[a,b] (ANSI/VITA)	**CompactPCI (PICMG 2.X)**	**CompactPCI Express (PICMG)**	**PXI (PXI System Alliance)**	**PXI Express (PXI System Alliance)**	**MTCA.0 (PICMG)**	**MTCA.4 (PICMG)**	**MTCA.4.1 (PICMG)**	**ATCA (PICMG 3.X)**
Applications	Industrial controls, telco, military, avionics, medical, transportation, simulations, general business, HEP	Industrial controls telco, telephony, data acquisition, military, avionics, surveillance, mission critical systems, HEP	Industrial controls telco, telephony, data acquisition, military, avionics, surveillance, mission critical systems, HEP	Industry, military, RF, communication, audio, video, testing equipment, instrumentation, data acquisition, and HEP	Industry, military, RF, communication., audio, video, testing equipment, instrumentation, data acquisition, and HEP	Industry, automation, teleco, military, instrumentation, avionics, nuclear physics, telemetry, mission critical systems, HEP	HEP, research, data acquisition, video processing, energy exploration, defence, homeland security, instrumentation, mission critical systems	HEP, research, data acquisition, video processing, energy exploration, defence, homeland security, instrumentation	Teleco, military, defence, instrumentation, aerospace, security, surveillance, industrial automation, data acquisition, mission critical systems, HEP
Maximum power per slot	35 W	35 W	35 W	3U 25 W 6U 50 W	3U 30 W 6U 60 W	80 W	80 W[c]	80 W[d]	600 W 800 W[e]
Front module size	3U/6U/9U[f] x 4 HP[g], 100 x 160 mm, 233 x 160 mm, 233 x 340 mm, 360 x 340 mm	Eurocard form factor, 3U/6U x 6 HP, 100 x 160 mm, 233 x 160 mm	Eurocard form factor, 3U/6U x 6 HP, 100 x 160 mm, 233 x 160 mm	3U or 6U, 100 x 160 mm, 233 x 160 mm	3U or 6U 100 x 160 mm, 233 x 160 mm	2U/4U x 4, 6, 8 HP Single width: 180 x 75 mm, Double width: 180 x 150 mm	4U x 6 HP, 180 x 150 mm	4U x 6 HP, 180 x 150 mm	8U x 6 HP, 280 x 322 mm
Rear module size	6U x 80 mm	3U or 6U, 100 x 80 mm, 233 x 80 mm	3U or 6U 100 x 80 mm, 233 x 80 mm	NA	NA	NA	4U x 6 HP, 180 x 150 mm	4U x 6 HP, 180 x 150 mm	8U x 6 HP 70 x 322 mm, 280 x 322 mm[h]
Maximum number of slots	21	31	31	31	31	12	12	12	14 (19”), 16 (23”), 32 (side B)
Power Supply	+5 V, +/-12 V, custom	+3.3 V, +5 V, +/-12 V	+3.3 V, +5 V, +/-12 V	+3.3 V, +5 V, +/-12 V	+3.3 V, +5 V, +/-12 V	+3.3 V, +12 V	+3.3 V, +12 V	+3.3 V, +12 V custom on RTM	+3.3 V, -40..-72 V

[a]VME eXtensions for Instrumentation System Specification (VXI) is an extension of the VME Bus specification dedicated for automated test instruments.
[b]VME-bus switched serial (VXS) is a ANSI/VITA standard using additional gigabit serial interfaces.
[c]The maximum 80-Watts power is available for both AMC and RTM modules. The AMC module should use maximum 50 Watts, whereas the RTM card could consume maximum 30 Watts.
[d]The AMC module could use maximum 80 Watts, whereas the RTM card consumes maximum 80 Watts provided via RF backplane.
[e]The double-height modules can support up to 800 Watts on single ATCA module (PICMG 3.7).
[f]Unit of vertical height defined in IEC 60297-1 corresponds to 44.45 mm (1.75 inches).
[g]Horizontal Pitch (HP) size corresponds to 5.08 mm (0.2 inch).
[h]Extended Transition Module (ETM) with second, rear-side backplane.

8) Running a final serial production:
   a) Verification of the electronic system and/or all electronic components of the system using an automated test-bench.
   b) Evaluation of performance and detailed tests of built system and its subsystems in a laboratory.
   c) Final verification of system parameters compliance with design requirements.
   d) Installation and integration of the electronic system and electronic system components with HEP machine.
9) Maintenance of the electronic control system of the HEP machine:
   a) Update of low- and high-level software.
   b) Periodic verification of subsystem parameters and calibration of subsystems.
   c) Verification of the electronic system using the management and diagnostic subsystem.
10) Upgrade of the HEP machine and electronic systems.

III. HARDWARE PLATFORM FOR HEP SYSTEMS

A part of the proposed methodology is a selection of suitable hardware platform that has direct influence on system reliability and performance. Therefore, it is important to select a flexible enough platform that assures both the required system availability as well as provides suitable processing power and allows for further extension or upgrade of the system.

A significant number of control systems applied in HEP is still designed with application of the ANSI/IEEE VME Bus (Versa Module Europa Bus) technology. The standard is based on the VME Bus that was developed more than 50 years ago for the 68000 family Motorola processors. The parallel bus makes it possible to send data via chassis backplane with maximum 320 Mbps data throughput using 32-bit data bus or 640 Mbps when 64-bit bus is applied. Selected parameters of the standard are presented in Table I.

The developed in the seventies specification does not allow to design powerful control and data acquisition systems used by modern physics. The main disadvantages are: a parallel bus

TABLE II
COMPARISON OF BACKPLANE INTERFACES FOR SELECTED STANDARDS

	VME Bus (ANSI/VITA)	CompactPCI (PICMG 2.X)	CompactPCI Express (PICMG)	PXI (PXI System Alliance)	PXI Express (PXI System Alliance)	MTCA.0 (PICMG)	MTCA.4 (PICMG)	MTCA.4.1 (PICMG)	ATCA (PICMG 3.X)
Data transport interface	VME bus[a], Master-Slave	32- and 64-bits PCI interface	StarFabric, Serial RapidIO, Serial Mesh, PCI Express, Serial ATA, Ethernet, USB	32- and 64-bits PCI	PCI Express	PCI Express, Ethernet, Storage Interfaces, Serial RapidIO, User defined	Ethernet, InfiniBand, StarFabric, PCI Express, Serial RapidIO, User defined	Ethernet, InfiniBand, StarFabric, PCI Express, Serial RapidIO, User defined	Ethernet/Fibre Channel, InfiniBand, StarFabric, PCI Express, Serial RapidIO, User defined
Data throughput	In range of Mb/s	In range of Gb/s	In range of tens of Gb/s	In range of Gb/s	In range of tens of Gb/s	In range of tens of Gb/s	In range of tens of Gb/s	In range of hundreds of Gb/s	In range of Tb/s
Backplane topology	Bus	Bus	Star, Dual-Star	Bus	Bus, Star	Star, Dual-Star	Star, Dual-Star, and Partial-Full-Mesh	Star, Dual-Star, and Partial-Full-Mesh	Dual-Star, Dual-Dual-Star, Full-Mesh, Replicated Mesh Fabric
Analogue and RF Signals	Front panel, not defined by standard	Front panel, not defined by standard	Front panel, not defined by standard	Front panel, not defined by standard	Front panel, not defined by standard	Front panel, not defined by standard	Front panel, Zone 3	Front panel, Zone 3, dedicated RF backplane	Not defined by standard
Trigger	NA	NA	NA	Star topology: 13 signals, Trigger bus: 8 signals	Star topology: 13 signals, Trigger bus: 8 signals	NA	Trigger bus: 8 signals	Trigger bus: 8 signals	No defined, could be implemented using fabric region
System Clock	Single VME clock: 16 MHz	Single PCI clock: 33 or 66 MHz	Single PCIe clock: 100 MHz +/-300 ppm	10 MHz +/-100 ppm	10 MHz +/-100 ppm, 100 MHz +/-100 ppm	3 clock signals (kHz to MHz)	3 clock signals (kHz to MHz)	3 clock signals (kHz to MHz)	3 clock signals (kHz to MHz)

[a]Further VME extenssion standards (e.g. VXS) supports also switched serial interfaces.

with low data throughput, high failure rate of the system, lack of built-in hardware management and diagnostics for modules installed in the chassis.

The standard requires dedicated computers, equipped with a VME Bus controllers that are nowadays hardly available and offer limited processing power. On the other hand, modern computers use a serial PCI Express interface for data transmission. Therefore, the VME-based systems need to use two interfaces: the legacy VME Bus and PCI Express or Gigabit Ethernet for fast data exchange. This complicates the architecture of the device, increases its cost, and reduces reliability of the whole system.

Various industrial standards suitable for complex systems are available such as: VME Bus, CompactPCI, CompactPCI Express, PXI, PXI Express, Compact RIO, AdvancedTCA, MicroTCA.0, MicroTCA.4 and MicroTCA.4.1 [2]–[4], [6], [7], [9], [21]–[29]. The comparison of selected hardware platforms taking into consideration their applications, electrical and mechanical parameters, is presented in Table I.

Modern computers, data acquisition, and control systems use serial interfaces with data throughputs reaching tens or hundreds of gigabits per second (e.g. 32 Gbps for 4 lane, gen. 3 PCI Express or 10/40/100/400 Gb Ethernet family). Most of the interfaces (data transmission, reference and RF clocks, trigger and interlock signals) are distributed on the chassis backplane in order to enhance the reliability of the system. The crucial signals applied in HEP (especially high-frequency analogue signals) should be connected from rear side of the chassis. Such a solution significantly simplifies system cabling, diagnostics and servicing. Various HEP system based on VME Bus specification use the serial gigabit interfaces available on front panels. This requires a distribution of significant number of additional cables and therefore has a negative influence on system reliability.

The historic VME Bus standard does not support power supply nor cooling redundancy. It is also not possible to use system management nor diagnostics. This prevents real-time hardware diagnostics during operation from predicting the incoming system failures, e.g. in power supply or cooling subsystem.

It is not possible to hot-swap damaged modules during operation of the system without the need to shut down the device. The failure in power supply or cooling circuit usually causes general and expensive break down of the whole system. The limitations of the VME Bus specification were clearly visible during designing of the LLRF control system of FLASH accelerator.

The system designed with this technology allows to control the FLASH accelerator, and therefore fulfils the basic functional requirements.

However, the system does not fulfil the non-functional requirements concerning reliability, scalability, and availability of the device.

For these reasons, the author started looking for new ways to design systems that meet HEP requirements. This includes searching for new hardware architectures suitable for devel-

TABLE III
COMPARISON OF PARAMETERS THAT COULD HELP TO IMPROVE SYSTEM AVAILABILITY

	VME Bus (ANSI/VITA)	CompactPCI (PICMG 2.X)	CompactPCI Express (PICMG)	PXI (PXI System Alliance)	PXI Express (PXI System Alliance)	MTCA.0 (PICMG)	MTCA.4 (PICMG)	MTCA.4.1 (PICMG)	ATCA (PICMG 3.X)
Platform Management, Diagnostics	NA	PICMG 2.9	PICMG 2.9	NA	NA	IPMI V.2.0	IPMI V.2.0	IPMI V.2.0	IPMI V.2.0
Hot-Swap	NA	PICMG 2.12	PICMG 2.12	NA	NA	AMC.0 PICMG 3.0	AMC.0 PICMG 3.0	AMC.0 PICMG 3.0	PICMG 3.0
Signal keying	Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying	Electronic/ Mechanical keying
Redundancy	NA	Data transmission	Data transmission	NA	NA	Management, Power supply, Cooling, Data transmission[a], Reference clock signals	Management, Power supply, Cooling, Data transmission, Reference clock signals	Management, Power supply, Cooling, Data transmission Reference clock signals	Management, Power supply, Cooling, Data transmission[b], Reference clock signals

[a]Dual Star topology with redundant hub module is supported.
[b]Base and Fabric data transport interfaces are available. Full Mesh, Dual Star and Dual-Dual Star topologies with redundant hub modules are supported in Fabric interface region.

opment of complex, distributed control and data acquisition systems.

The comparison of available backplane interfaces, data throughputs and connection topologies is presented in Table II, whereas table III summarises parameters that have a direct influence on system reliability, including platform management, diagnostics and possible redundancy.

From HEP point of view, particularly the xTCA standards: Micro Telecommunications Computing Architecture, Advanced Telecommunications Computing Architecture and Advanced Mezzanine Card are interesting. The collection of interoperable xTCA standards that supports hot-swap technology, power supply, cooling and data transmission redundancy allow to design high-reliability, scalable telecommunications systems [1]–[4], [6], [7], [9], [21]. The AdvancedTCA technology makes it possible to build systems with 99.999% availability and therefore fulfils the reliability and scalability requirements of HEP devices [2]. The main disadvantage of the AdvancedTCA is the high price of the components and lack of recommendations indicating how to construct mixed analogue-digital systems that are applied in HEP. The standard is well suited for very complex systems processing data from thousands or tens of thousands detectors. On the other hand, the MTCA.0 specification prevents to design complex control systems because of a small size of AMC modules (85 x 180 mm) [7], [9]. Only, the new MicroTCA.4 (MTCA.4) standard developed in 2011 [3], that takes advantage of double width AMC and RTM (Rear Transition Module) cards, enables the design and implementation of the LLRF system. All xTCA standards support easy expandability and upgradeability, including in-system firmware upgrade.

It is worth mentioning, that the xTCA standards have been designed to build complex digital systems for telecommunication applications. The standards lack information and guidance on how to design analogue systems such as data acquisition and control systems of high-energy physics. The PCI Industrial Computer Manufacturers Group is currently working to standardize the auxiliary MTCA.4 backplane dedicated for distribution of high frequency RF analogue signals and reference low phase jitter clock signals (MTCA.4.1 specifications) [4]. The migration of analogue RF signals to a separate backplane allows to obtain better parameters of the system, such as temperature stability, noise performance, etc.

The MicroTCA.4 specification seems to be well suited for HEP applications. The standard offers 12-slot chassis supporting front (AMC) as well as rear site (RTM) modules with IPMI hardware management and diagnostics, possibility of power supply, cooling tray or connectivity redundancy [30]. The main disadvantage of the standard is maximum four lanes fat-pipe backplane interface that limits data throughput to maximum 32 Gbps for PCIe x4 in generation 3 and to 40 Gbps for Ethernet[3].

Further, research conducted by the author has shown that the MicroTCA.4 standard seems to be well suited even for complex and demanding control and data acquisition systems. It provides the opportunity to obtain better control parameters and reduce the cost of building the entire LLRF control system. The use of redundancy in power supply, cooling, the build-in management, and diagnostic subsystems allows to increasing system availability and therefore make the technology attractive for HEP applications.

IV. EXAMPLE SYSTEMS THAT FOLLOW THE METHODOLOGY

The methodology proposed by the author for the design of data acquisition and control systems as well as the results of his research have been used to design control systems of free electron lasers, such as Free-Electron Laser in Hamburg, the European X-ray Free Electron Laser and diagnostic systems of an ITER experimental thermonuclear reactor.

The first prototypes of the FLASH and EXFEL LLRF systems were built using the AdvancedTCA standard. How-

[3]PICMG is currently working on the AMC.2 40 Gbps Ethernet specification.

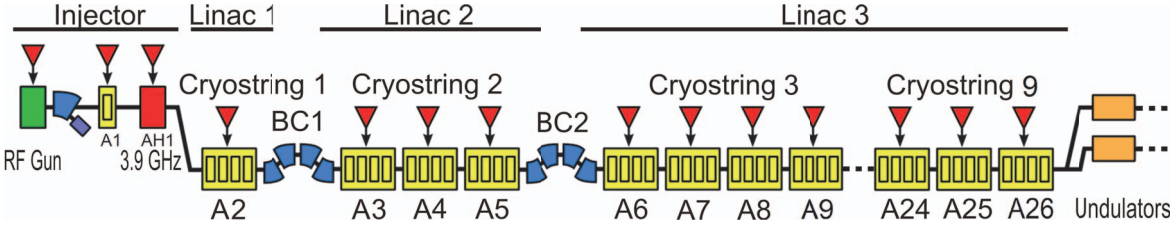

Fig. 1. The layout of the European XFEL accelerator

ever, the final LLRF system was designed using the MTCA.4 specification when the work on the PICMG standard was finished.

Further research conducted by the author has shown that the use of the new MTCA.4 standard provides the opportunity to obtain better control parameters and reduce the cost of building the entire LLRF control system.

The developed methodology is currently used by the Department of Microelectronics and Computer Science for the implementation of the system compensating Lorentz force detuning of the ESS (European Spallation Source) accelerator cavities within the Polish in kind contribution[4].

A. LLRF Control System of XFEL Accelerator

The European X-ray Free Electron Laser is the 4^{th} generation synchrotron light source that is capable of producing high-intensity ultra-short wavelength X-ray laser light [31], [32]. EXFEL is composed of an electron accelerator section and undulators that emit coherent laser light. The layout of the EXFEL accelerator is presented in Figure 1 [16].

The linear accelerator is composed of 808 superconducting cavities operating with 1.3 GHz frequency. A single RF (Radio Frequency) station in the accelerating section consists of four cryogenic modules (total 32 cavities) and it is supplied from a single 10 MW klystron. The accelerating section, counting 100 cryo-modules, is controlled by 26 RF (Radio Frequency) sections (A1–A26 as presented in Figure 1).

The selected functional and non-functional requirements for the LLRF system of the EXFEL accelerator:

1) Precision of acceleration field regulation in amplitude and phase: $\Delta A/A_{(rms)} < 0.01\%$ and $\Delta\phi < 0.01\circ$ for 1.3 GHz frequency signal respectively.
2) Minimization of power required for nominal operation.
3) Modular and scalable system architecture.
4) High availability, serviceability and upgradeability.

LLRF system electronics is installed in the accelerator tunnel and therefore it is exposed to gamma radiation and neutron influence [33]. Therefore, the design of the system need to guarantee and proper operation in such conditions.

The first prototype of the LLRF system was developed with AdvancedTCA standard [10]–[15], [34]. Despite the fact that the AdvancedTCA architecture has many advantages, it does not seem to be well suited for LLRF system applications. The architecture of the system was not optimal. The biggest problem was poor analogue performance and significant distortions of high-frequency analogue RF signals. At this time author started research concerning the HEP design methodology. Further research resulted in the design of the new promising LLRF system developed in MicroTCA.4 form-factor.

The LLRF system is composed of 51 MicroTCA.4 master- and slave-chassis distributed within 1.5 km long accelerator tunnel [35], [36]. A single RF station (master and slave chassis) processes data from 32 cavities and generates the klystron drive signal. Down converter modules (DWC) are fabricated as RTM cards that are connected to the digitizer (ADC) cards designed as AMC modules. The slave module transmits a partial vector sum (VS34) to the digital controller Master module, which calculates the total vector sum of the gradient of accelerating cavities and generates a signal driving the vector modulator VM [16], [18], [19]. All RF stations are synchronised to Master Oscillator (MO) generator. The layout of the MicroTCA.4 master chassis in presented in Figure 2.

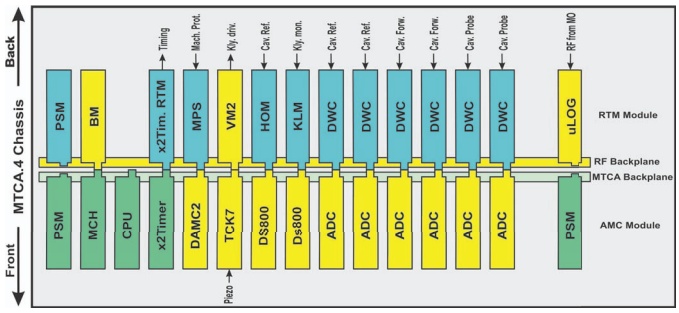

Fig. 2. AMC and RTM modules installed in the MicroTCA.4 chassis of the European XFEL LLRF system (Master system).

The LLRF system components are currently being commissioned at DESY [37]. The preliminary results prove that the LLRF control system of the EXFEL accelerator is able to regulate the acceleration RF field with $\sigma(dA/A) = 0.056\%$ (pulse-to-pulse regulation) and theretofore fulfils the requirements.

B. Image Acquisition System

Diagnostic systems of ITER tokamak will use more than 200 digital cameras working in the visible, infrared, and gamma radiation range [38]. The imaging system should acquire and process data from cameras with the resolution of 1 to 8 million pixels registered within the range of 50 to 50000 frames per second [20].

A single digital 1 megapixel camera registering image with a framerate of 1000 frames per second generates a stream of data exceeding 8 Gb/s[5] [20], [39]. Therefore, the imaging

[4]The in-kind contribution made by the Polish Electronic Group (PEG) consortium consisting of the Lodz University of Technology, the Warsaw University of Technology and the National Centre for Nuclear Research.

[5]Assuming 8 bits for a single pixel.

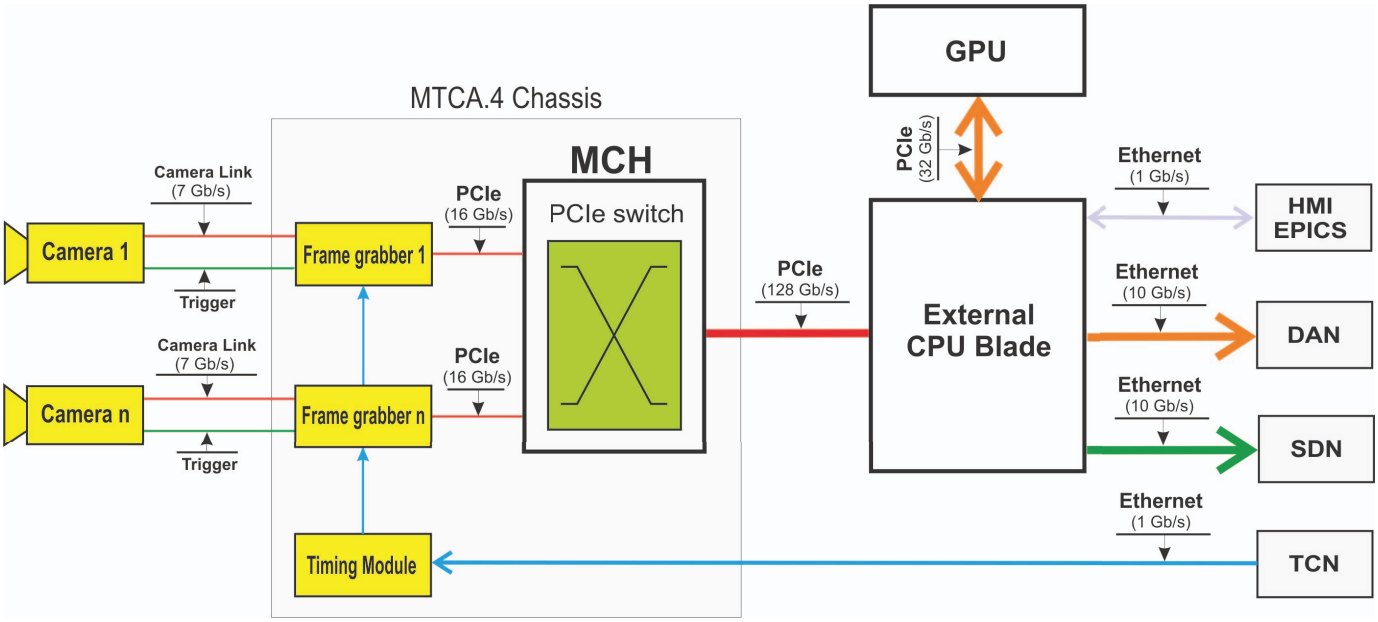

Fig. 3. A block diagram of Image Acquisition and Processing System developed according to the proposed methodology

system needs to process a large amount of data in real-time. The total data stream for such system could reach 1.6 Tbps assuming the same parameters (1 megapixel, 1000 fps) for all digital cameras.

All devices should be synchronised with an accuracy better than 50 ns (rms) [40]. Processing of megapixel images with 1000 fps in real-time requires an application of powerful computation units [41], [42]. Critical, real-time algorithms should be processed with low latency using Field Programmable Gate Array (FPGA) devices, whereas more complex algorithms could be computed with CPU or GPU [43]–[45]. It is desired that the system should use redundancy in power supply, cooling subsystems and image processing path in order to enhance its reliability.

It is worth mentioning, that the electronics of diagnostic systems will be installed in the area with increase magnetic field (ca. 30 mT) and radiation. Therefore, the system needs to tolerate both the increased magnetic field and radiation [38].

The IAS prototype was designed and built with MicroTCA.4 standard according to the proposed methodology. During development of system architecture various limitations of MicroTCA.4 specification were identified. Large processing power CPUs cannot be used because of the limited maximum power dissipated in a single chassis slot (up to 80 W). The other restriction is the 4-channel FatPipe bus (ports 4-7 on the backplane) that limit the maximum CPU data throughput to 32 Gbit/s (PCIe x4, gen. 3). Similar constraints concern GPU accelerators. At this stage the architecture of the system was modified. A large processing power external CPU with additional GPU card were applied instead of the internal MicroTCA.4 CPU. The developed PCI Express link to external CPU allows to overcome the limitations of MicroTCA.4 technology [46]. The block diagram of the designed MicroTCA.4-based IAS is presented in Figure 3.

The proposed, completely new architecture of the image acquisition and processing system, enabled the data processing with maximum data throughput up to 1 terabit per second [20], [46]. A single MicroTCA.4 chassis could accommodate up to 11 frame grabber cards[6] and therefore acquire image stream from many cameras. It is possible to use the GPU accelerator installed in an external computer.

Currently tested system enables to transfer data from the MTCA.4 chassis to the external computer 4 times faster (128 Gbps) than in the case when the computer is inside the chassis (32 Gbps) [46]. It is possible to increase the bandwidth even further up to 1 Tbps when PCIe in generation 4 will be applied and the computer will be connected via 4 links. Part of the PCIe connection to external CPU could be used in redundant way. It is also possible to use two external CPUs each connected with two redundant data channels to a single MicroTCA.4 chassis. Such a solution allow to easily adapt the computation power and the required level of redundancy that has a direct influence on system reliability.

The methodology allows to design a scalable and powerful imaging system that fulfils the requirements for ITER diagnostic systems.

V. Conclusions and Plans for Future

A methodology for developing complex systems used in HEP was proposed by the author. The methodology helps to choose a suitable hardware platform for the system and guides the designer during the whole designing and implementation process.

The methodology was verified during the development of the complex distributed LLRF system for EXFEL accelerator and the final production of AMC and RTM modules. The electronic components are installed in the accelerator tunnel directly under the accelerating cryostring and therefore are exposed to gamma radiation and neutron influence. The developed control system has a scalable construction. The design

[6]A single slot is reserved for timing module.

takes advantages of modularity, redundancies and hot-swap functions offered by the standard. The IPMI management and diagnostic subsystems allows for a real-time diagnostics.

The production of modules was realised in two stages: trial and final production. In both cases, the production and evaluation of modules was straightforward. The initial tests proved that the LLRF system fulfils the specification.

A suitable hardware platform to design a powerful and scalable image acquisition system, that meets the ITER requirements, has been selected using the proposed methodology of designing complex systems for HEP.

The methodology helped to identify the restrictions of MicroTCA.4 technology at early stage and choose a suitable architecture for the system. Such a system, composed of tens of MicroTCA.4 chassis, could acquire and process images from hundreds of high-resolution digital cameras. The proposed architecture could also find efficient applications in industry sector.

The developed methodics and proposed hardware architectures can be also applied to build other systems used in physics experiments. A good example is the European Spallation Source accelerator currently being constructed at Lund in Sweden. The Lorentz force detuning system is developed in a MicroTCA.4 form-factor according to the design rules presented in this paper.

The methodology could be further modified and adopted for other applications that require efficient data processing and improved reliability, including industry, military and space exploration.

Various diagnostic systems of ITER tokamak will be developed and installed by 7 Domestic Agencies (DAs). It is a real-challenge to assure compatibility between the subsystems provided by various countries and to guarantee the proper operation of the whole tokamak. The author in cooperation with ITER experts develops a new methodology for designing, integrating, and testing the tokamak diagnostic subsystems provided by various DAs [47].

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